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Design of a FPGA-based controller for power and period measurement in the start range of Dalat Nuclear Research Reactor

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Abstract: This paper introduces a new controller module based on a high-speed field-programmable gate array (FPGA) and digital signal processing (DSP) using moving average (MA) filters for calculation of the reactor power and period at the start range of the Dalat nuclear research reactor (DNRR). The reactor power is proportional to the neutron flux in the reactor core, and the reactor period is the time that the reactor power changes by a factor of 2.718. In the control and protection system (CPS) of the DNRR, the reactor power and period have been monitored by the 8-bit microprocessor controller named BPM-107R. There are two main functions of the BPM-107R controller including 1) measurement and determination of reactor power and period and 2) generation of warning and emergency protection signals by reactor power or/and by reactor period. Those discrete signals will access to the logical processing unit of the CPS to prohibit the upward movement of control rods or to shut down the reactor. The CPS has three BPM-107R controllers corresponding to three independent neutron flux measurement equipment (NFME) channels working by logic voting "2 out-of 3". Each NFME channel was designed for detection of neutron flux density in the full range from 1×10^0 to 1.2×10^{10} n/cm^2×s, which is divided into two sub-ranges named start range (SR) and working range (WR). The designed FPGA-based controller module was tested using simulated signals as well as signals from the CPS in comparison with the original controller BPM-107R. The experimental results show that the characteristics and functions of the two controllers are equivalent.

Keywords: *Reactor period, reactor power, moving average filter, FPGA, DSP.*

I. INTRODUCTION

The reactor power (P) and reactor period (T) are parameters directly related to safety operation of a nuclear reactor. In reactor operation condition, the time rate of power change is very important, particularly at the start-up stage, then monitoring the reactor period is an effective way to prevent the reactor power from increasing rapidly. Therefore, the on-line and accuracy calculations of reactor power and period have been required to avoid uncertain shutdown or nuclear incidents.

In case of the CPS of DNRR, when the reactor power is greater than P_{preset} by 10% (P_{preset} can be set from 1% to 100% of 500 kWt by 1% step) or the period is less than 20 s, the emergency protection signal EMR-P or EMR-T will be generated to shut down the reactor and hold it at a subcritical state by inserting neutron-absorbing control rods into the reactor core. The above-mentioned functions have been realized by the existing

embedded micro-controller BPM-107R using DS87C530 processor. Main characteristics of this controller include the working clock frequency is of 30 MHz, the data memory (RAM) is of 32 kbyte, the programme memory (ROM) is of 64 kbyte and the length of each neutron parameter generation cycle is of 200 ms [1, 2].

The digital CPS of the DNRR was designed and supplied by the SNIIP SYSTEMATOM JSC of Russia and put into operation in 2007. It was the second generation of the instrumentation and control (I&C) system for nuclear reactors that was designed by this JSC, meanwhile, the fifth generation of I&C system has been operated at some nuclear reactors since 2015. As usual, after 13 years of operation, many functional electronic modules of the CPS were out of products in the market for spare parts and replacement. Besides, taking into accounts on the advantage of the FPGA technology for design and construction of nuclear electronic equipment, nowadays fast integrated FPGA-based devices are widely developed for measurement, data storage and acquisition system in nuclear physics experiments and nuclear engineering, such as for radiation measurements with high resolution X-ray spectroscopy with pulse height analyzer [3], for readout systems of the cosmic ray angular distribution based on flash analog-to-digital converter using FPGA technology [4], and for nuclear data measurement by (n, γ) and (n, 2γ) reactions at horizontal experimental neutron beam ports of nuclear research reactor with high performance gamma spectrometers [5]. Considering the above-mentioned reasons and propensity, the main purpose of this work is to develop the new FPGA-based controller module which can be a spare-part or replacement for the BPM-107R controller when necessary. The developed controller applies DSP principle with moving average filtering technique using a Xilinx FPGA Artix-7 with on-board clock of 50 MHz and two 32-bit counting channels that can sample and calculate reactor power pulse signals every 20 ms. Some comparisons with the current BPM-107R controller module were performed by simulated signals as well as by real signals from neutron detectors of the start range.
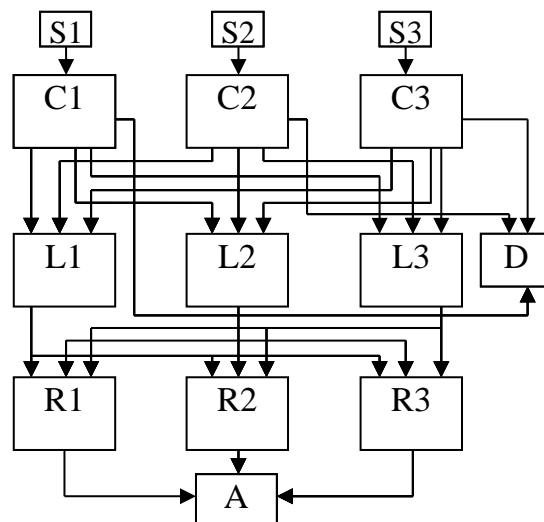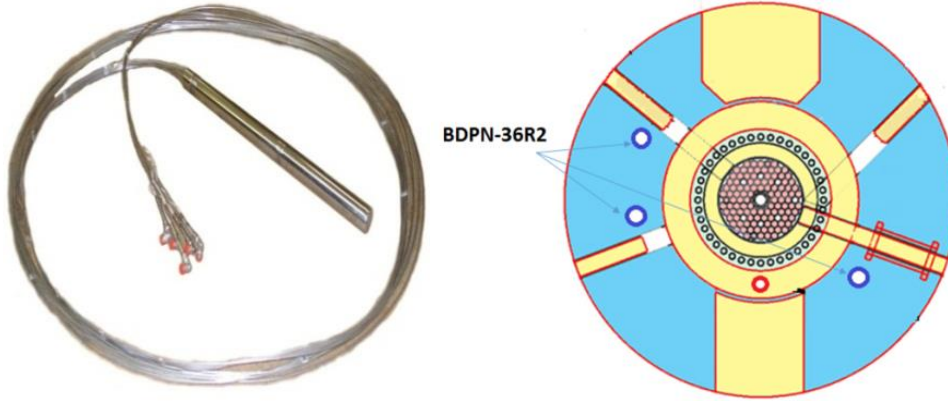

Fig. 1. The "2 out-of 3" data processing and architecture of the DNRR' CPS
(S – sensor/detector, C – Controller, L – Logic processing, R – Relay block, A – Actuator,

The CPS of DNRR is operating based on "2 out-of 3" principle as shown in Fig. 1. Three neutron detectors are installed in dry channels outside the reactor core, as shown in Fig. 2.

**Fig. 2.** Neutron detector unit BDPN-36R2 (left) and detector locations in reactor pool (right)

II. METHODS

A. Nuclear reactor power and period caculation

Neutron density (power) of a nuclear reactor follows the exponential function of:

$$P(t) = P_0 e^{\frac{t}{T}} \qquad (1)$$

Where, P(t) is transient reactor power at time t, P_0 is initial reactor power at time t_0, T is the time taken for the power to change by a factor e (e = 2.718 which is the base of natural logarithm) that called the reactor period, t is time during the reactor transient.
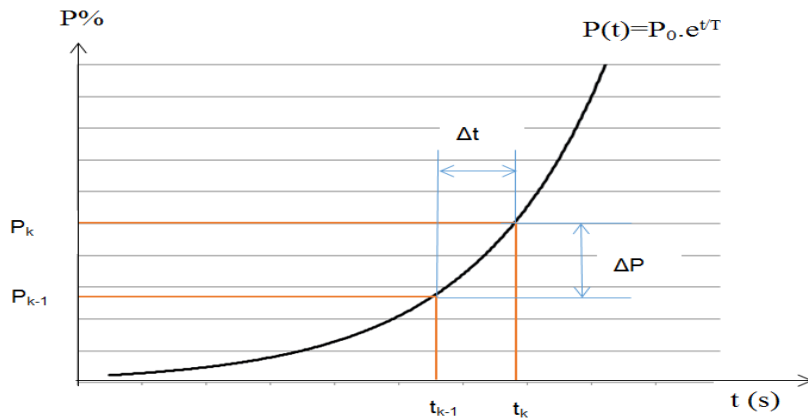
Fig. 3. Sampling for nuclear reactor power and period calculation

To calculate the reactor period from (1), it is necessary to convert continuous time models as Fig. 3 to discrete time form, using finite difference techniques. The reactor period in digital nuclear instrumentation system can be calculated by the equation (2) [6]:

$$T = \frac{1}{\frac{dP}{dt} \times \frac{1}{P}} \text{ or } \frac{1}{T} \approx \frac{\Delta P}{P \Delta t} \approx \frac{P_k - P_{k-1}}{P_k} \times \frac{1}{\Delta t} \text{ or }$$

$$T = \frac{P_k}{P_k - P_{k-1}} \times \Delta t \qquad (2)$$

Where, P_{k-1}, P_k is the (k-1)-th and k-th sampled reactor power, $\triangle t$ is the sampling period in seconds.

From equation (2) we can see that the reactor period can reflect the state of a nuclear reactor. When $P_k - P_{k-1} = 0$, the reactor is in a stable state (T ⌣ 999 s); when $P_k - P_{k-1} > 0$, the reactor power increases; and when $P_k - P_{k-1} < 0$, the reactor power decreases. The reactor period can be monitored from 0 to 999 s by 1 s step.

The reactor power level is proportional to the reactor neutron flux, therefore, the output frequency from a pulse amplifier is proportional to the reactor power level, then the relationship between the reactor power at the start range (P_{SR}) and the output frequency of the pulse amplifier can be calculated as:

$$P_{SR} = K_{SR} \times F_{SR} \times 10^{-6} \qquad (3)$$

Where, P_{SR} is the reactor power at the start range, K_{SR} is a coefficient, F_{SR} is the output frequency from the pulse amplifier which is connected to the fission chamber for monitoring in the range from 10^{-6} to 10^{-1} % $P_{nominal}$ ($P_{nominal} = 500$ kWt).

B. Design of moving average filters using FPGA and DSP

A moving average (MA) filter is a type of finite impulse response filter (FIR)

[7]. It is used widely in many applications in digital signal processing, communications, control, electrical and biomedical systems. The main purpose of MA filter is to increase the signal to noise ratio and to reduce random noise.

A simple moving average (SMA) filter is a filter that averages N points of previous inputs and makes an output with them, the formula is expressed as follows: [8, 9]

$$\bar{P}_{SM} = \frac{P_M + P_{M-1} + ... + P_{M-(n-1)}}{n} = \frac{1}{n}\sum_{i=0}^{n-1} P_{M-i}$$

(4)

When calculating sequential values, a new value comes into the sum, and the oldest value moves out, n is coefficient or window of filter. Equation (4) can be rewritten as:

$$\bar{P}_{SM} = \bar{P}_{SM,pre} + \frac{1}{n}(P_M - P_{M-n}) \qquad (5)$$

Where, $\bar{P}_{SM}$ is the average value, $\bar{P}_{SM,pre}$ is the previous average, P_M is the new sample, P_{M-n} is the n-th old sample, n is the window of SMA filter.

Equation (5) can be described in Fig. 4, in which the reactor power and the reactor period are calculated by DSP technique embedded on FPGA.
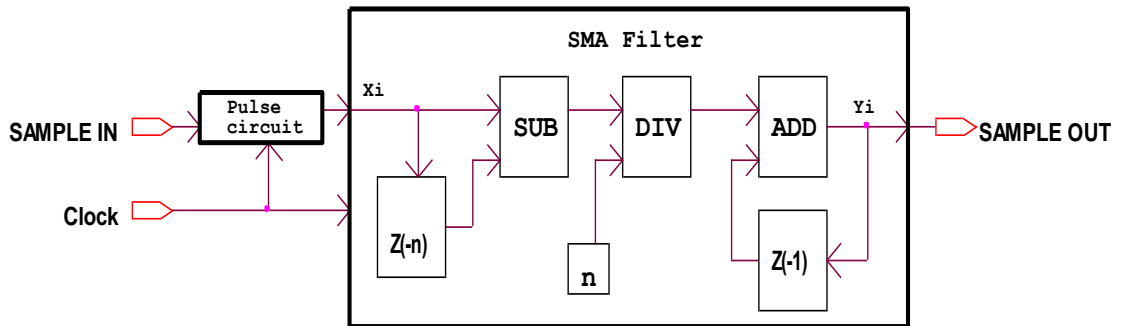

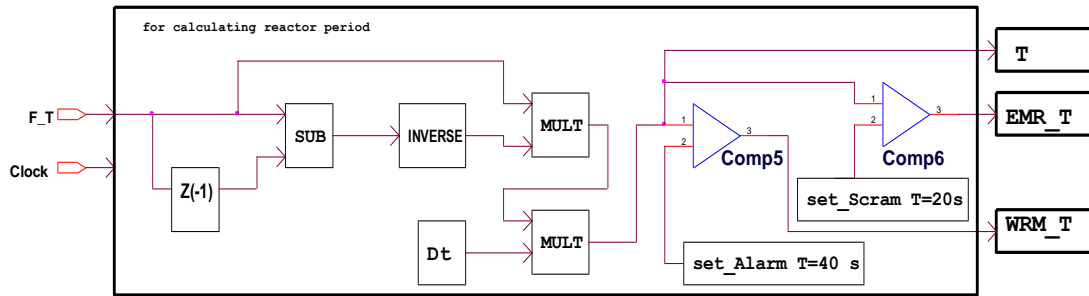**Fig. 4.** Principle schema used for moving average filter

Fig. 5. Principle schema used for calculating reactor period

SAMPLE IN is the input of the SMA filter that is processed by a pulse circuit for normalizing the pulse width, then counting, accumulating and performing SMA filtering technique, the output signal (SAMPLE OUT) is frequency, n is a coefficient of filter that is dependent on the fluctuation of input signal.

The diagram for reactor period calculation by Eq. (2) can be described in Fig. 5.

F_T is the output signal from SMA filter that is used for calculating reactor period, and then calculated period is compared with set_Alarm T (40 sec) and set_Scram T (20 sec) to generate discrete signals WRN_T and EMR_T, respectively. Further, these signals will access to the logical processing unit of the CPS, in which signal WRN_T is used for formulation of a command to prohibit the upward movement of control rods, meanwhile EMR_T signal formulates a command to shut down the reactor.

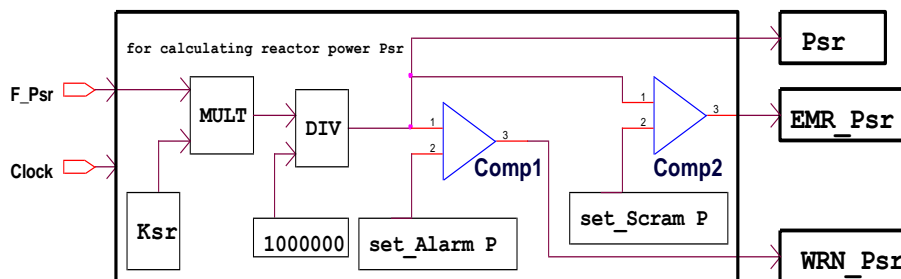To calculate the reactor power at the start range, Eq. (3) is described in Fig. 6.

Fig. 6. Principle schema used for calculating reactor power at start range

As shown in Fig. 6, the F_Psr signals are performed to calculate the reactor power for the start range (Psr). Then these values are compared with set_Alarm P (5% P_{preset}) and set_Scram P (10% P_{preset}) for generating discrete signals WRN_Psr and EMR_Psr, respectively. Further, these discrete signals will access to the logical processing unit of the CPS, in which signal WRN_Psr is used for formulation of a command to prohibit the upward movement of control rods, meanwhile EMR_Psr signal formulates a command to shut down the reactor.
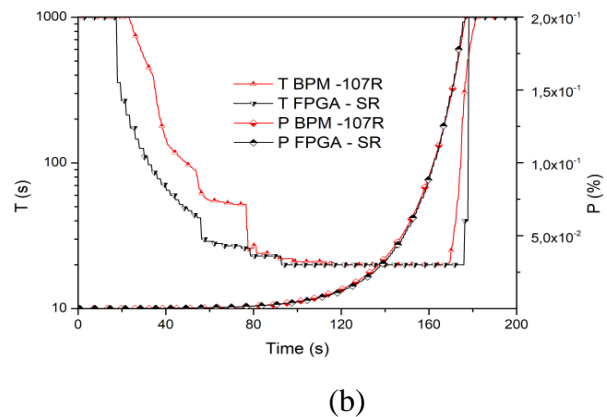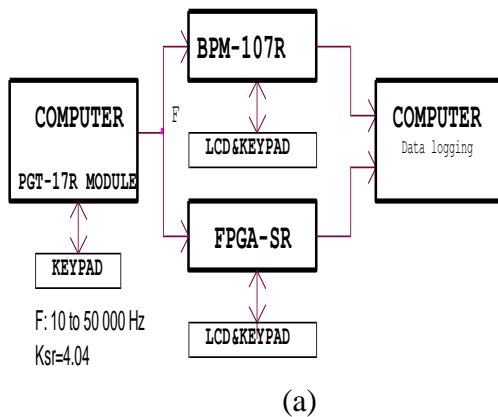
III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Testing of the designed controller in the start range by simulator

The simulator module PGT-17R, designed by SNIIP SYSTEMATOM JSC, was used for testing of the new designed controller module in the start range (named FPGA-SR). The experiment which was setup

to measure the power and the period for testing FPGA-SR and BPM-107R controllers is shown in Fig. 7(a). The values of power and period of both the controllers were recorded (data logging) using a computer via Terminal v1.9b software.

In the CPS, the K_{SR} coefficient for calculating reactor power was calibrated to be 4.04. The initial value of simulated frequency was 10 Hz and the final value was 50,000 Hz. The simulated period was chosen to be 20 s.

The relative error of the monitored reactor power in the range from 4×10^{-5} to 2×10^{-1} % $P_{nominal}$ is within 5% and that of the monitored reactor period is within 10%, which are reported in [10]. Figure 7(b) shows the testing results for period measurement at 20 s by the BPM-107R and FPGA-SR controllers. The period curve of the BPM-107R controller reaches to 20 s slower than that of the FPGA-SR controller, in which the period curve reaches to 20 s only after about 100 s.

Fig. 7. Principle schema for measurement of power and period using PGT-17R simulator module (a) and Testing results of BPM-107R and FPGA-SR controllers using PGT-17R module with F_{SR} from 10 Hz to 50,000 Hz at 20 s period (b)

The main reason of different results between two controllers is due to their different architectures. The BPM-107R controller is based on the 8-bit DS87C530 microprocessor operating with 30 MHz clock frequency that can sample and calculate reactor power pulse signals between 20 ms to 200 ms. Meanwhile, the new developed controller is based on the high speed FPGA with 50 MHz on-board clock and two 32-bit counting channels that can sample and determine the above procedures every 20 ms. The other reason is that in the range of reactor power lower than 5×10^{-4} % $P_{nominal}$, the statistic counting of simulated pulses is still very low, therefore, in order to achieve the ideal curve from 5×10^{-4} % $P_{nominal}$ (from this value the emergency protection is started monitoring), the filter coefficient in the BPM-107R was changed as jumping steps. Instead of that, the coefficient n (or window) of SMA filters in the FPGA-SR controller with embedded DSP circuits can be flexibly changed to achieve the such ideal curve.

Fig. 7(b) also shows that both the BPM-107R and FPGA-SR controllers give almost the same results in the case of simulation for power measurement.

B. Testing of the designed controller by neutron signals in start range of the reactor

The experimental schema to measure the reactor power and period at the CPS using neutron signals from neutron detectors in the reactor is shown in Fig. 8.
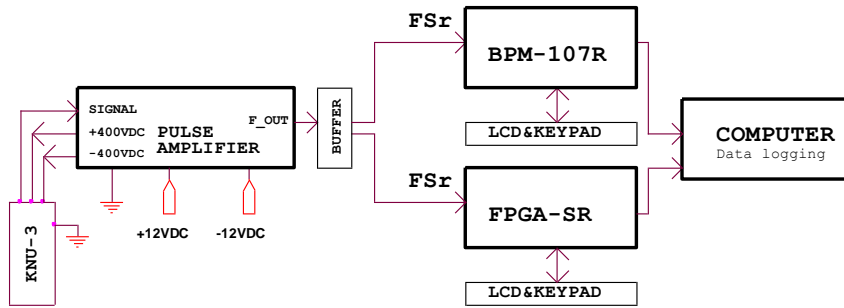
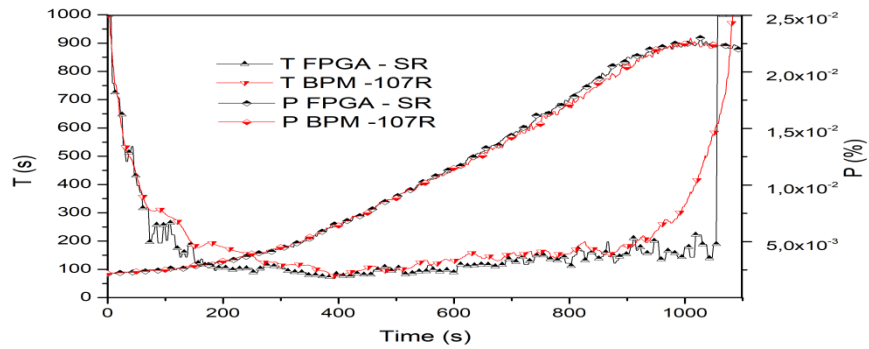**Fig. 8.** Principle schema for measurement of reactor power and period

Fig. 9. Results of reactor power and period measurement by FPGA-SR and BPM-107R controllers in the range from 4×10^{-5} to 2×10^{-2} % $P_{nominal}$
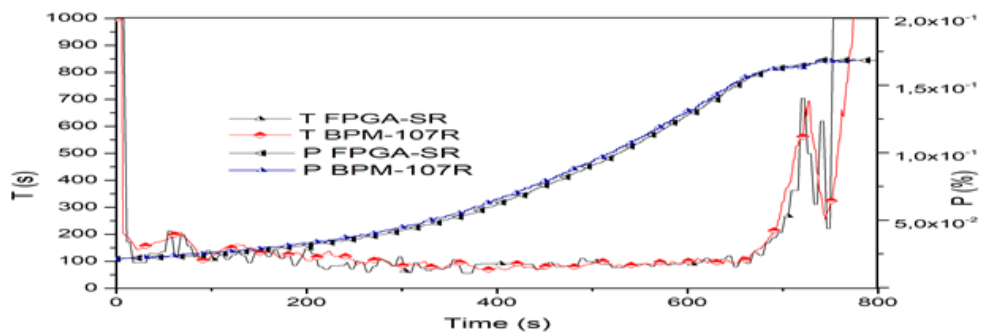

Fig. 10. Results of reactor power and period measurement by FPGA-SR and BPM-107R controllers in the range from 10^{-2} to 2×10^{-1} % $P_{nominal}$

The start range was designed for monitoring the reactor power in the range from 4×10^{-6} to 2×10^{-1}% $P_{nominal}$. In practice, the lowest power level is about 4×10^{-5} % $P_{nominal}$ due to epithermal and fast photoneutrons, which are produced by the $^{9}Be(\gamma, n)2$ ^{4}He and $^{9}Be(n, 2n)2$ ^{4}He reactions, respectively, are significant in the reactor core, especially when the reactor operates frequently.

Fig. 9 and Fig. 10 show the results of the reactor power and period measurement in the range from 4×10^{-5} to 2×10^{-1}% $P_{nominal}$ by the FPGA-SR and BPM-107R controllers. The results show that both the controllers have almost the same value.

As mentioned above, in case of the FPGA-SR controller, the coefficient n of SMA filters can be flexibly changed, so its response time is faster than that of the BPM-107R controller as shown in Fig. 7(b).

IV. CONCLUSIONS

Based on the application of DSP technique with moving average filters embedded on FPGA, the functional circuits for the controller module have been designed for measuring and determining the reactor power, the reactor period, and generating the protection signals whenever the value of the reactor power or period is beyond the preset threshold value.

The developed FPGA-based controller was tested in comparison with the BPM-107R module of the CPS, which was designed by SNIIP SYSTEMATON JSC of Russia. The testing was performed both by pulse-generated simulator PGT-17R and by real neutron signals from the reactor. The experimental results of measuring reactor power and period by the FPGA-SR and BPM-107R controllers indicate a good agreement of their functions and characteristics, including the reactor power measured in the range from 4×10^{-5} to 2×10^{-1} % $P_{nominal}$ with the accuracy less than 5% and the reactor period is monitored in the range from 1 to 999 s with the accuracy less than 10%. Additionally, the emergency protection signal EMR-P or EMR-T is generated, when the reactor power is greater than P_{preset} by 10% or the period is less than 20 s.

The obtained results also permit to conclude that the new developed FPGA-based controller meets the design purposes and can perform all functions of the existing BPM-107R controller, therefore, it can replace the BPM-107R controller when needed.

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